EGC220 Practice Problems for Exam 2

Circle T (true) or F (false) for each of these Boolean equations.

(a). T (F) An 8-to-1 multiplexer requires 2 select lines.
(An 8-to-1 multiplexer requires 3 select lines).

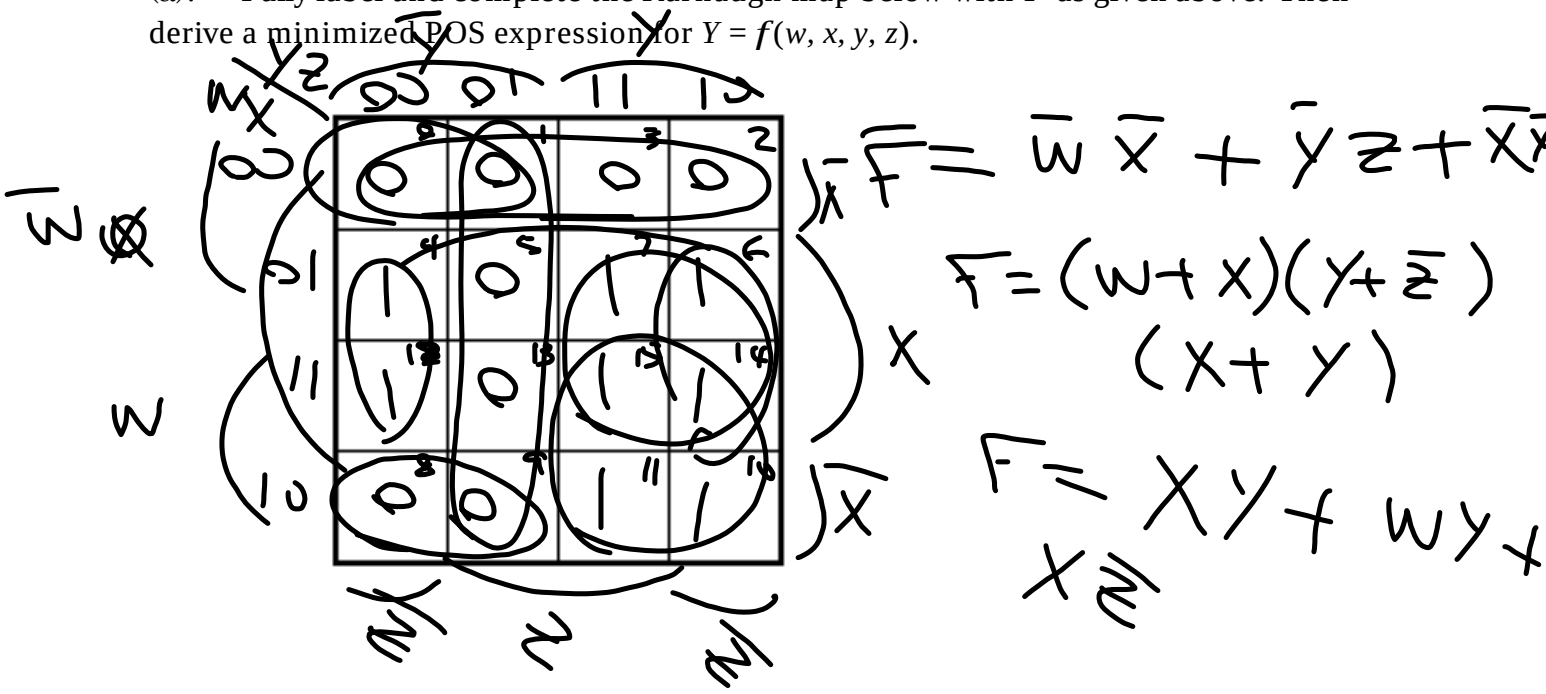
(b). T (F) A half adder has a carry input.
(A half adder has no carry input).

(c). (T) F Even parity means the data has an even number of bits that are 1.

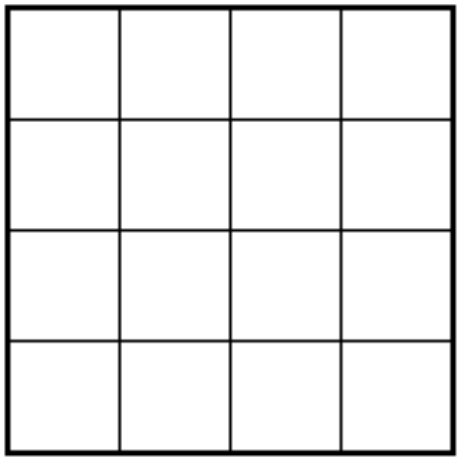
(d). T (F) If a decoder has 16 outputs, it requires 3 inputs to choose all possible outputs.
(A 16-output decoder requires 4 inputs to choose all outputs).

2. For $Y = f(w, x, y, z) = \Pi M(0, 1, 2, 3, 5, 8, 9, 13)$

(a). Fully label and complete the Karnaugh map below with Y as given above. Then derive a minimized POS expression for $Y = f(w, x, y, z)$.



(b). Fully label and complete the Karnaugh map below with Y as given above. Then derive a inimized SOP expression for Y.



3. Combinational Logic:

Design a circuit that counts the number of 1's present in 3 inputs A, B and C. Its output is a two-bit number X_1X_0, representing that count in binary. Assume active-HIGH logic.

3(a). Write the truth table for this circuit.

Solution:

A	B	C	X_1	X_0
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

3(b). Find the minimized logic equations for outputs X_1 and X_0; use a K-map if needed.

Solution:

A K-map for X_0 is not very helpful, as it results in 4 isolated minterms, $\overline{A}\,\overline{B}\,C + \overline{A}\,B\,\overline{C} + A\,\overline{B}\,\overline{C} + ABC$. However, we may recall from the binary adder lab that this equation can be factored further using the XOR operator $\oplus$.

Factor out $\overline{A}$ and A from their respective terms to obtain:

$X_0 = \overline{A}(\overline{B}C + B\overline{C}) + A(\overline{B}\,\overline{C} + BC) = \overline{A}(B \oplus C) + A(\overline{B \oplus C}) = A \oplus (B \oplus C)$.

$X0 = A \oplus B \oplus C$

K-Map for X_1:

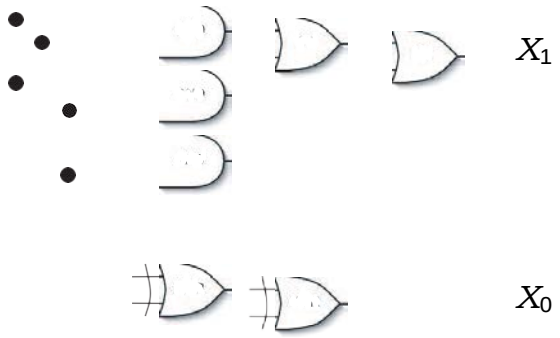
A	00	01	11	10
0	0	0	1	0
1	0	1	1	1

SOP expression for $X1$: blue vertical pair=BC
green horizontal pair=AC, red horizontal pair=AB

$X1 = AB + AC + BC$

3(c). Draw the corresponding logic diagram for this circuit. Label all inputs and outputs.

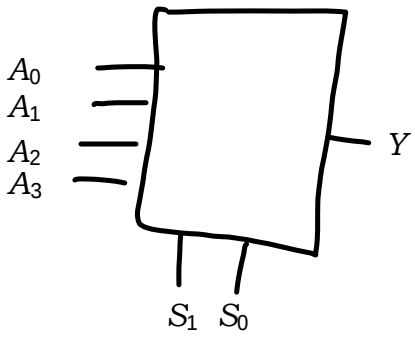
A B C



4. Combinational Logic: Multiplexers and Encoders

4(a). Draw a block diagram of a 4-to-1 multiplexer. Do not use a gate-level diagram. Label all inputs and outputs.

Solution:



S_1	S_0	Y
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

$Y = \bar{S}_1 \bar{S}_0 A_0 + \bar{S}_1 S_0 A_1 + S_1 \bar{S}_0 A_2 + S_1 S_0 A_3$

4(b). Draw a block diagram of a 4-to-2 encoder. Label all inputs and outputs. How is the 4-to-2 encoder different from a 4-to-1 multiplexer?

Solution:

The 4-to-2 encoder has 4 input lines and 2 output lines. Only one input line should be active at a time. The 2 output lines send the 2-bit binary number corresponding to which input line is active. So if line A_1 is active, the output Y_1 Y_0 will be 01.

The 4-to-1 multiplexer has 4 input lines, and 2 select lines. The 2 bits from the select lines choose the input line which will be used as output, so the data sent on that input line will be output. So if the select lines S_1 S_0 = 01, whatever data is on input line A_1 will be output on Y.

4(c). Write the truth table for a 4-to-2 priority encoder. Write a simplified truth table for a 4-to-1 multiplexer (hint: your multiplexer truth table should have 2 inputs).
Solution:
Truth Table for 4-to-2 priority encoder:

A_3	A_2	A_1	A_0	Y_1	Y_0
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

Truth Table for 4-to-1 multiplexer:

S_1	S_0	Y
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

5. Combinational Logic: Binary Adders

You wish to add two 4-bit numbers. You have half adders and full adders available to use as components.

5(a). Draw a block diagram of your 4-bit adder, using half and full adders. Do not draw a gate-level diagram. Show and label all inputs and outputs.

Solution: